

WHAT IS CLAIMED IS

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1. A semiconductor integrated circuit,
comprising:

pads;

10 a first power supply I/O cell which is
connected to an external pin through a corresponding
one of said pads; and

15 a second power supply I/O cell which is
not connected to an external pin through a
corresponding one of said pads, but receives power
supply from said first power supply I/O cell.

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2. The semiconductor integrated circuit as
claimed in claim 1, further comprising:

an internal cell;

a power supply line which provides power
supply to said internal cell;

25 a line which connects between said first
power supply I/O cell and said power supply line;
and

30 a line which connects between said second
power supply I/O cell and said power supply line.

35 3. The semiconductor integrated circuit as
claimed in claim 1, wherein said second power supply
I/O cell is not connected to the corresponding one
of pads that corresponds to said second power supply

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I/O cell.

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4. A method of designing a power supply layout of a semiconductor integrated circuit, comprising the steps of:

10 identifying an unused I/O cell having no external connection; and

assigning the I/O cell to be a power supply I/O cell having no direct external connection.

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5. The method as claimed in claim 4, further comprising a step of connecting the power supply I/O cell to a power supply line for providing
20 power supply to an internal cell and connecting the power supply I/O cell to a power supply I/O cell having direct external connection through a pad.

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6. The method as claimed in claim 4, further comprising a step of identifying a portion that is lacking in a power supply current inside a
30 chip, wherein said step of assigning the I/O cell assigns the power supply I/O cell with respect to said portion.

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7. The method as claimed in claim 6,

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wherein said step of identifying a portion that is lacking in a power supply current includes the steps of:

- obtaining first information about
- 5 assignment of pins to I/O cells;
- obtaining second information about an
- amount of a necessary power supply current needed at
- each position inside the chip;
- calculating an amount of a provided power
- 10 supply current in an initial state based on the
- first information; and
- comparing the calculated amount of a
- provided power supply current with the amount of a
- necessary power supply current indicated by the
- 15 second information.

- 20 8. The method as claimed in claim 4,
- wherein said step of assigning the I/O cell includes
- a step of identifying the I/O cell to be assigned by
- use of a pointing device on a screen display that
- presents an illustration of a chip.

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- 9. The method as claimed in claim 4,
- 30 wherein said step of assigning the I/O cell includes
- a step of identifying the I/O cell to be assigned by
- specifying a number that has been allocated on the
- chip.

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10. A semiconductor integrated circuit,
made by a designing process that comprises:
identifying an unused I/O cell having no
external connection; and
assigning the I/O cell to be a power
supply I/O cell having no direct external connection.

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